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Wafer Saw Process Optimization for Die Chipping Mitigation on Extremely Small Leadframe Package

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

The paper focused in addressing the silicon die chippings defect at the wafer sawing process of an extremely small semiconductor package. In-depth potential risk analysis and Pareto diagram were done to identify the top reject contributors and eventually resolve the issue. A comprehensive design of experiment (DOE) was done and validation of the solution was employed to formulate the effective corrective actions. Results revealed that die chippings were addressed by optimizing the wafer sawing process through enabling the dressing, pre-cut and step-cutting modes. Ultimately, an improvement of 95% for die chippings reduction was achieved.

Keywords: Wafer saw; pre-cut; step-cut; die chipping.

1. INTRODUCTION

New trends and continuous development in semiconductor technology offer great challenges in assembly manufacturing industry. An imperative challenge for any industry is to sustain its competitive market value and position. Important to note that failure to provide customer expectation in terms of quality and time-to-market speed would result to probable business

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failure. This unfavorable scenario should really be avoided that is why a line-stressing or risk production is being employed in preparation to full or mass production mode.

The device in focus on this paper is a newly introduced leadframe package in the plant having an extremely small footprint as illustrated in Fig. 1. The device functions as a diode with a single-wire connection, for computer and mobile applications. Regardless of its simple geometry, it is considered as a device with high complexity since advanced platforms are required to satisfy its output process.

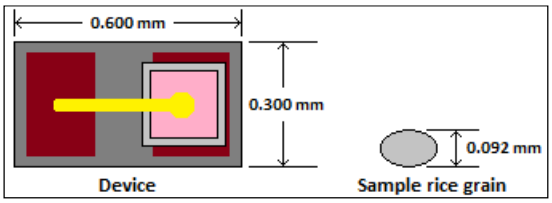


Fig. 1. Device dimension

The device has a very thin die and packaged in an extremely small footprint. The assembly process includes a step-cutting method of wafers which is not common on other semiconductor industries. Assembly process flow applicable to the device in focus is shown in Fig. 2. Worthy to note that assembly manufacturing process flow varies with the product and its technology [1-3]. With the continuous technology development and introduction of state-of-the-art platforms, challenges in semiconductor assembly manufacturing are inevitable [4-6].

Assembly issues were encountered during the line-stressing and ramp-up of the device. Critical processes were categorized using risk analysis, and one of which is identified in Table 1 which focused on the critical wafer sawing process. Evaluation was employed before the risk build to fast-track confidence on line-stressing. In addition, potential risk analysis was given contingency plans and corrective actions were created.

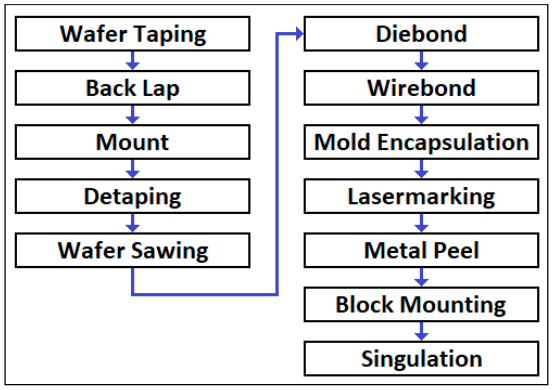


Fig. 2. Assembly process flow

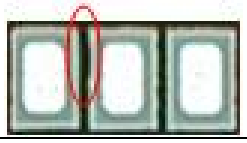
Reject contributors on the pin-pointed critical processes are given in Fig. 3. Wafer saw is one critical process identified with output abnormalities or deviations as a result of non-optimized parameters. Note that the deviations are normally attributed to newly introduced products or devices.

Of the 23% defect contribution of the wafer sawing process, Pareto diagram in Fig. 4 shows die chippings as the top reject parts per million (ppm) contributor. Note that criteria for rejects are governed by assembly process specifications and work instructions [7,8]. Machine parameter optimization is one of the factors to be investigated as the device in focus has no similar product in the plant as reference. Benchmarking for comparable device from other sites is being considered to have a reference or baseline for critical process parameters.

Table 1. Potential risk analysis at wafer saw process

Identified risk	Resulting potential risk	Evaluation before action			Identified action
		Probability	Impact	Class	
Wafer sawing quality (conductive die-attach film adhesion, die chippings, small dice dimensions, excessive dice-off)	▪Low yield ▪Reliability	9	9	A	Sawing process using step-cut method, wafer staging

Table 2. Top defect signature wafer saw process

Critical process	Top Defect signature	Criteria	Remarks
Wafer saw	Die chippings 	Not allowed to reach active metallization	Failed

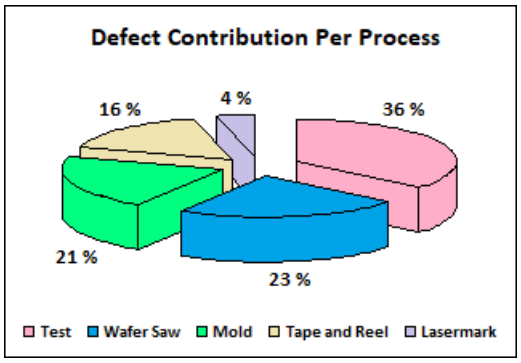


Fig. 3. Defect per process contribution

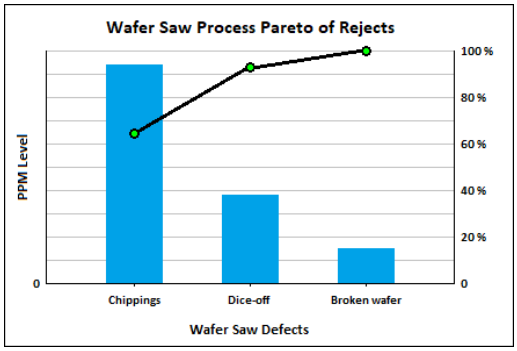


Fig. 4. Pareto diagram of wafer saw rejects showing the top contributor

Top rejects based on Pareto diagram significantly affect the yield and delivery during production stressing performance. With this, process optimization is highly recommended at line-stressing, before it reaches the full production release. Table 2 shows the top defect signature of the wafer saw process. Further analysis and investigation of failures are completed by collecting actual reject samples on this critical process. Corrective actions are then formulated.

2. REVIEW OF RELATED LITERATURE

The device in focus has a very thin and low-K (a material with a small dielectric constant) wafer, making the sawing a critical process. When abrasive blades groove or cut the material, they are in fact grinding and removing it. The mechanism is like that of a metal saw. The gaps, called chip pockets, between the teeth of the saw whisk material away from the point of processing as highlighted in Fig. 5.

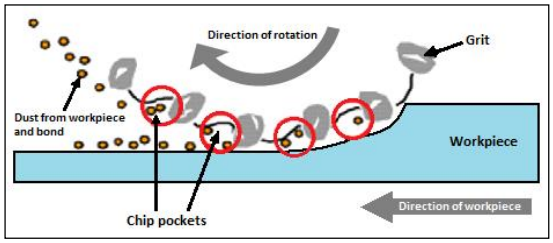


Fig. 5. Chip pockets occurrence during wafer sawing process

New blades have diamonds covered wholly by the bonding material and no diamonds are exposed on the surface, hence, diamonds cannot make cracks [9]. If the wafer is cut with this condition, big chippings would happen, or the blade would be broken depending on the cutting speed. After dressing, bonding material is removed and diamond comes out on the surface and small hole called chip pocket is created at the same time. Chippings are normally present on a new blade, therefore, blade dressing and pre-cut are needed to be performed. Note that blades are dressed before shipment. Nevertheless, pre-cut operation is needed to condition the blade and eventually minimize occurrence of chippings.

Note that dressing and pre-cutting cannot simply eliminate chippings when using a single blade. Single blade carries a greater process load, thus, resulting to an increase in surface chippings. This is the reason why a step-cutting mode using two blades (Z1 and Z2) shown in Fig. 6 was introduced to minimize chippings during wafer cutting or sawing. Z1 blade would partially cut the wafer then Z2 totally cuts the wafer, making it a stress-relief process.

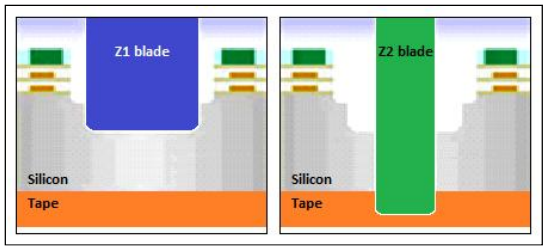


Fig. 6. Wafer saw step-cutting method

3. METHODOLOGY

To address the die chipping occurrence, design of experiment (DOE) in Table 3 was done on the three input variables of wafer saw process: dressing, pre-cutting, and step-cutting modes.

Table 3. Evaluation matrix for wafer saw process

Process	Run 1	Run 2	Run 3	Run 4	Run 5
Dressing	Yes	Yes	No	No	Yes
Pre-cut	No	Yes	Yes	No	Yes
Step-cut	No	No	Yes	Yes	Yes

A full factorial design with a total of nine runs was created and done. Results of each run are discussed in the succeeding section.

4. RESULTS AND DISCUSSION

Wafer saw process optimization was done and optimum parameters were attained based on the results of the DOE, addressing the top reject contributor of this critical process. Comparative tests were used to statistically validate the results with the aid of a statistical system software. DOE results confirmed that when blade is dressed, done pre-cut and used step-cutting mode, it would give the minimal surface chippings. Fig. 7 shows the analysis of variance (ANOVA) with all-pairs Tukey-Kramer test indicating a significant difference on Run 5 amongst the other runs in terms of die chippings.

After the implementation of the identified solutions, level of rejections was monitored. Fig. 8 shows the improvement in the ppm level, before and after the solution implementation.

An improvement of 95% for die chippings reduction was achieved through the comprehensive DOE. Assembly yield trend stabilized after the implementation, optimization, and sustainability of the improvement and all corrective actions. The performance improvement is a good indication of manufacturing preparedness for full production mode.

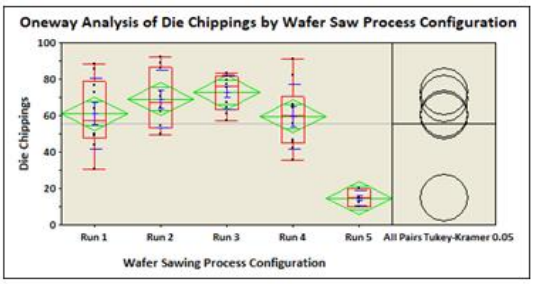


Fig. 7. Statistical analysis of variance indicating significant difference on Run 5

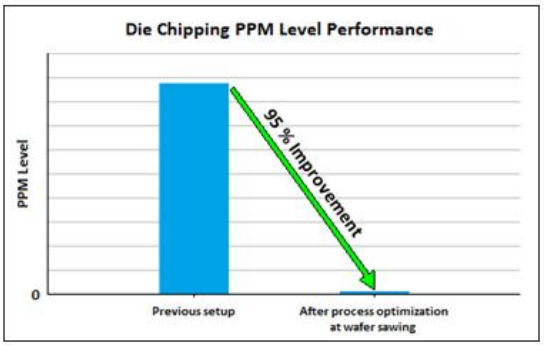


Fig. 8. Improvement after optimization and implementation of the corrective actions

5. CONCLUSION AND RECOMMENDATIONS

Comprehensive engineering analysis with the support of statistical analysis was done in solving and addressing the die chipping issue of an extremely small device at wafer sawing process. Through DOE, parameters optimization was formulated, with die chipping occurrence significantly minimized by doing dressing, pre-cut and step-cutting mode. A 95% improvement for die chippings reduction was ultimately achieved.

Although a flawless new package introduction cannot be attained immediately, process optimizations play critical role as early as line-stressing stage, before full or mass production release can be granted. It is highly important that when new devices are coming in, critical processes are needed to be identified and that proper corrective actions and solutions be employed so that when full production are set, quality and speed will both be achieved.

Moreover, studies and improvement done in [5,10,11] are helpful in reinforcing robustness and optimization of pre-assembly processes.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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