Journal of Engineering Research and Reports

12(3): 1-5, 2020; Article no.JERR.55992
ISSN: 2582-2926

Tool Setup Improvement for Package Scratch Mitigation at End-of-Line Process

A. Sumagpang Jr.[1*], F. R. Gomez[1] and R. Rodriguez[1]

[1]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna 4027, Philippines.

Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed, and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2020/v12i317079
Editor(s):
(1) Dr. Harekrushna Sutar, Indira Gandhi Institute of Technology, India.
(2) Dr. Pierre-Olivier Logerais, Université Paris-EstCréteil, France.
(3) Dr. P. Elangovan, Sreenivasa Institute of Technology and Management Studies, India.
Reviewers:
(1) Seah Choon Sen, Universiti Tunku, Malyasia.
(2) Raheel Muzzammel, University of Lahore, Pakistan.
Complete Peer review History: http://www.sdiarticle4.com/review-history/55992

Original Research Article

Received 22 February 2020
Accepted 30 April 2020
Published 06 May 2020

ABSTRACT

With new and continuous semiconductor technology trends, challenges in assembly manufacturing are inevitable. This paper focused on the elimination of assembly defects particularly package chip-out and scratch at the singulation end-of-line (EOL) process of a semiconductor device. Simulation using computer-aided design (CAD) tools, actual process replication, and validations were done, eventually verifying and replicating the desired defect signatures. Singulation tool setup of the package was improved and a standardized tool setup was established based on the simulation and actual validations, resulting to at least 90% improvement in assembly EOL process parts per million (ppm) reduction.

Keywords: Package scratch; chip-out; end-of-line; singulation; assembly.

1. INTRODUCTION

In the semiconductor manufacturing industry, package scratch and chip-out are common defects usually encountered in trim and form (T/F) process. For the device in focus of this paper, top defect incurred during assembly manufacturing was the package chip-out and/or

**Corresponding author: Email: antonio.sumagpang@st.com;*

scratch located at the top surface of the package, as shown in Fig. 1. In this scenario, the end-of-line (EOL) process parts per million (ppm) and its non-conformance report are high. This paper focused on addressing these assembly issues through process replication and with the help of package design simulation.

2. EXPERIMENTATION

The defect signatures were captured during the singulation stage at the T/F process. Fig. 2 shows the process mapping of the assembly reject. Worthy to note that assembly manufacturing process flow varies with the product and the technology [1-4]. With new and continuous technology trends and breakthroughs [5-7], challenges in semiconductor assembly manufacturing are unavoidable.

Package scratch and chip-out trend recovered in assembly yield and issues monitoring shown in Fig. 3 indicates significant failure for assembly EOL processes in a span of several months. High level of defect ppm occurrence was recorded during this time, affecting the assembly yield performance for this particular device. This triggered the team to deep dive onto the problem, identify the root-causes, and come-up with the best solution.

The singulation punch in T/F process guides and holds the package units to singulate or cut into individual units from the leadframe matrix. Punch applies a certain external force to the package and holds the unit to singulate. Punch requires a critical dimension in order to perform its required function. Fig. 4 shows how the unit is being singulated in case the singulation punch does not comply with the required dimension. Note that the assembly package design is governed by internal specifications and work instruction documents [9,10].

Aside from singulation punch dimension requirement, the singulation tool setup dimension is considered to be critical. Fig. 5 illustrates some portions of the singulation tool that requires dimension standards.

3. RESULTS AND DISCUSSION

3.1 Simulation and Validation of Package Defects

Actual validation was made with dimensions based on the modelling approach using a computer-aided design (CAD) tool. The original setup dimensions were simulated in the worst-case condition of punch location to replicate the package defect signatures as previously given. In Table 1, the simulation showed that the clearance between the punch and the lifting insert results in the bumping of the unit on the track entry and in the dislocation of the unit on the track during the ejection process.It also showed that the unit was dislocated, and the response of the package replicated the defect signature.

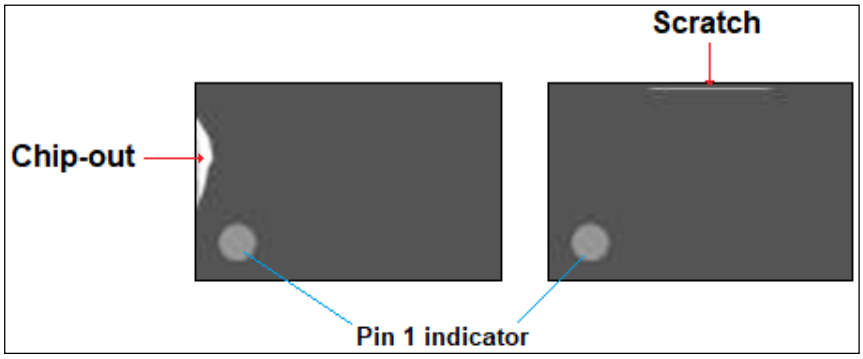


Fig. 1. Package chip-out and scratch

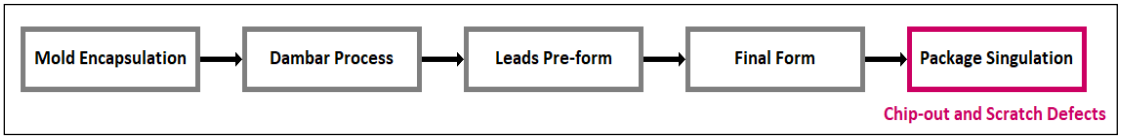


Fig. 2. Assembly process mapping

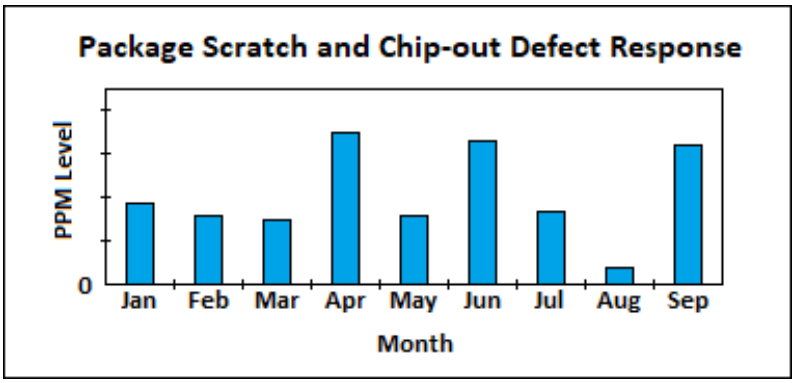


Fig. 3. Defect ppm response [8]

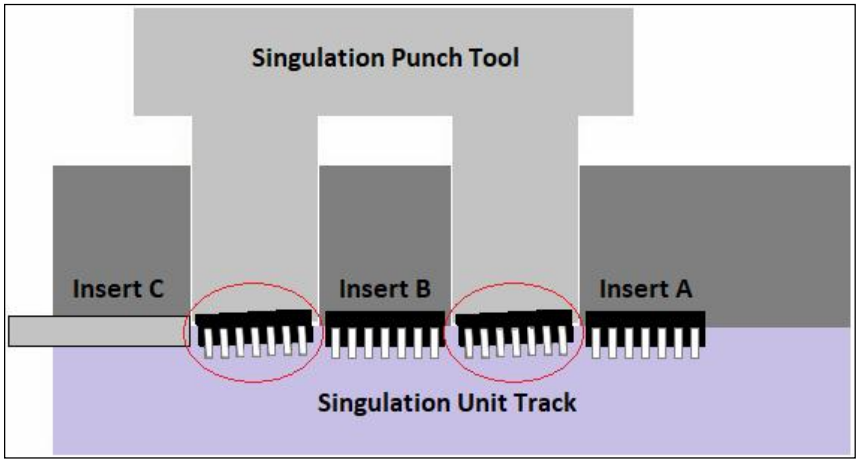


Fig. 4. Risk of mis-alignment during package singulation [8]

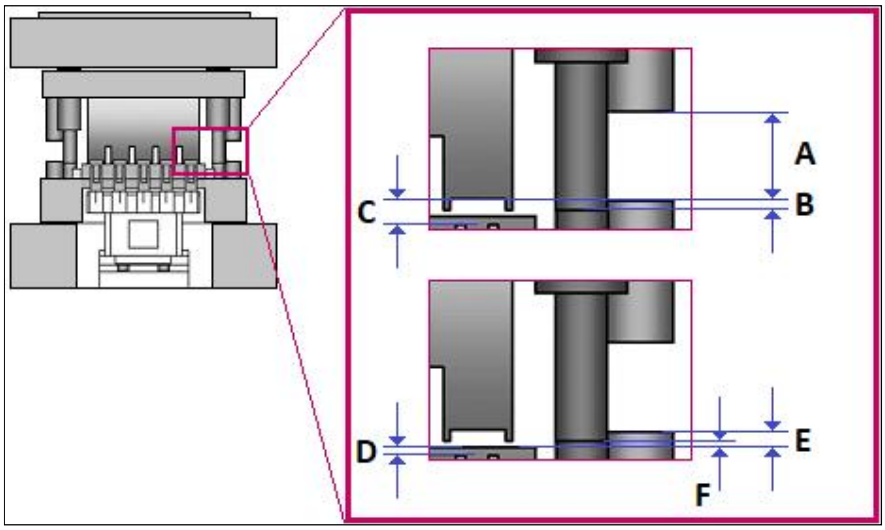
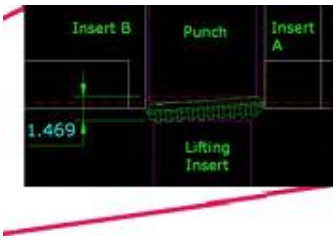


Fig. 5. Critical setup dimensions of singulation tool

Table 1. Simulation and actual replication of defect

Worst position setup condition	Computer simulation	Actual validation
		Defect signature   Actual package response

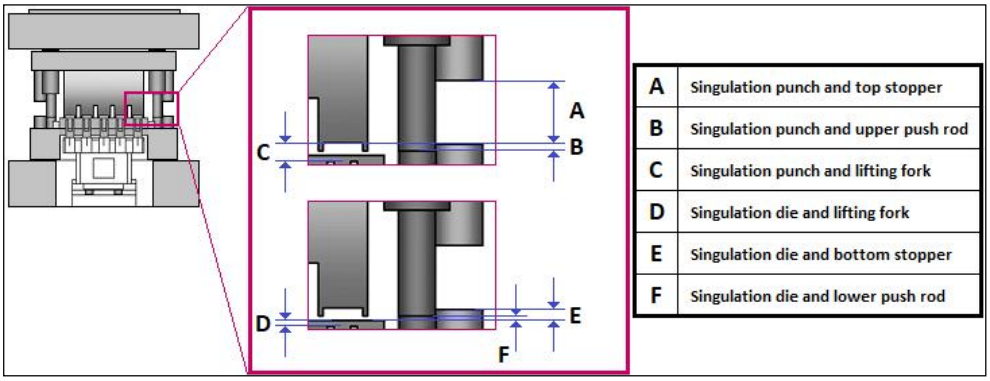


Fig. 6. Optimized and standardized singulation clearance setup

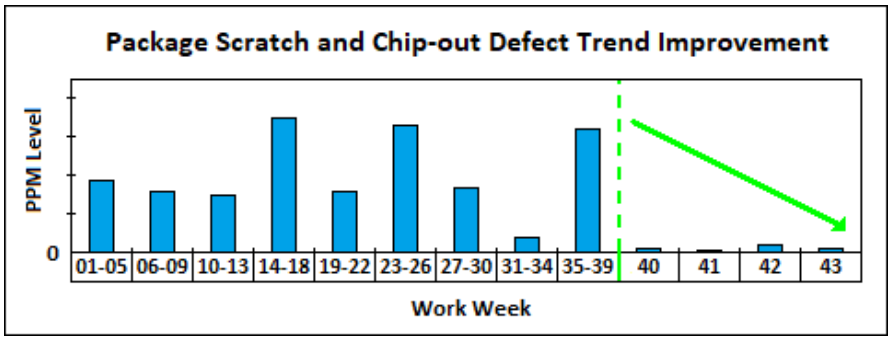


Fig. 7. Defect ppm trend improvement

3.2 Singulation Tool Setup Standardization

A standard and optimized dimension setup was established and standardized for the singulation tool. Fig. 6 shows the standard clearance setup of singulation tool to eliminate package anomalies particularly the chip-out and scratch defects.

3.3 Assembly PPM Trend Improvement

Based on assembly EOL process ppm and non-conformance report data, the simulation/replication made via design modification and singulation tool clearance standardization contribute a significant improvement for eliminating package scratch and chip-out, as highlighted in Fig. 7. A 90% improvement in assembly EOL process ppm reduction was achieved.

4. CONCLUSION AND RECOMMENDATIONS

The established standard and improved singulation tool setup of critical clearance significantly improved the assembly EOL process performance with average of 90% improvement in terms of ppm reduction of package scratch and package chip-out occurrence. The improved tool setup should be maintained and sustained to reduce and mitigate the said failures. One significant factor is the parts consumable replacement based on the wear and tear life condition set, requiring proactive ways to maintain the best quality and performance of the singulation tool.

It is recommended that improvement and corrective actions be sustained by understanding the wear and tear of the material via tool life identification for frequent parts replacements and maintenance. Another thing to consider is the tool clearance dimensional setup that can be attained by an appropriate die-setting dimensional inspection.

ACKNOWLEDGEMENTS

The authors would like to thank the New Product Development & Introduction (NPD-I) team and the assembly team who have greatly contributed to the success of the work. The authors are greatly thankful to the Management Team for the extended support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA; 2016.
2. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
3. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; October; 2004.
4. Geng H. Semiconductor manufacturing handbook. 2nd Ed., McGraw-Hill Education, USA; 2017.
5. Sumagpang A, Gomez FR. Challenges and resolution for copper wirebonding on tapeless leadframe chip-on-lead technology. Journal of Engineering Research and Reports. 2018;3(2):1-13.
6. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling.10th Electronics Packaging Technology Conference, Singapore;2008.
7. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan;2002.
8. Sumagpang A, Gomez FR. Specialized singulation punch design for package chip-out elimination. Journal of Engineering Research and Reports. 2019;5(2):1-7.
9. STMicroelectronics. Design rules manual for metal leadframe. rev. 4.0; 2018.
10. STMicroelectronics. Assembly and EWS design rules for wire bond Interconnect dice. rev. 53.0; 2018.

© 2020 Sumagpang et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/55992