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A Proposed Modified Constant Frequency Variable Duty PWM Based Speed Control Technique for DC Motor Drives: A New Method to Achieve More Precise Control over Speed

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Authors' contributions

This work was carried out in collaboration between all the authors. Author AA has carried out the entire design of the proposed system. Finally he has written the paper. Authors P. Sen, EC, P. Sarkar, NB, RD and ARM have carried out most of the experimental measurements presented in this paper. Authors AA, NB, RD and ARM helped to revise the paper according to the reviewers' comments. Author SC helped to sketch the PCB layout of the designed circuit. Author TKS has guided the group till the completion of the entire work. All authors read and approved the final manuscript.

Original Research Article

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ABSTRACT

In this paper, the authors have proposed a new method for speed control of DC motor drives via modified constant frequency-variable duty (CFVD) pulse width modulation (PWM) technique. The armature of the DC motor rotating in very low speed has to accept abrupt mechanical shocks (kicks) due to the application of large amplitude narrow pulse trains (very low duty cycle) while the speed of the DC motor is controlled by using the conventional CFVD PWM method. These consecutive abrupt mechanical shocks lead to reduction in life of the DC motor. In the proposed method, an extra control signal (having modified sinusoidal form) is subtracted from the conventional fixed amplitude CFVD PWM signal to obtain the modified speed control signal, which provides gradual periodic increase and decrease in the amplitude of consecutive pulses for all duty cycles. Thus for very low duty cycles (for achieving very low speed) the abrupt mechanical shocks on the

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armature can be avoided. Moreover, the peak amplitude of the subtracted extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the conventional PWM signal. A circuit for generating the modified control signal has been designed and also fabricated for testing. Finally the experiments are carried out to study the speed control characteristics of a 9 V DC motor drive. The proposed method is found to be better than the conventional CFVD PWM speed control method as regards flexibility in speed control, transient response and abrupt electrical breaking.

Keywords: Pulse width modulation; DC motor; chopper control; duty cycle; modified CFVD PWM; electronic breaking; transient response.

1. INTRODUCTION

Pulse width modulation (PWM) which is synonymous with pulse duration modulation (PDM) is a commonly used technique for the speed of DC motor drives [1-4]. The average value of the voltage and current fed to the DC motor can be controlled by turning an electronic switch between the supply and motor on and off at a fast pace. Longer the switch is on as compared to the off periods, higher the average voltage applied across the motor. Since the speed (in rpm) of a DC motor is directly proportional to the average voltage applied across it, thus by varying the supplied average voltage by means of variable on time period of the electronic switch, the speed of the DC motor can be controlled. The term 'duty cycle' is the ratio of the on time to the regular interval to the total time period. A low duty cycle corresponds to low power, since the supplied power is off for most of the time and vice versa. The PWM switching frequency has to be much faster than the response time of an electromechanical load such as DC motor drives. Typically from a few kHz to tens of kHz switching speed is used to control the speed of a variable speed DC motor drive [5]. The primary advantage of PWM based speed control is that, the power loss in the switching devices is almost negligible as compared to the losses in the linear supplies [6].

Over the last few years, several researchers have proposed various advanced techniques for speed control of motor drives [7-12], but PWM technique of speed control of DC motors are still the most popular and simplest one. PWM based speed control techniques are also sometimes called chopper control which are more power efficient, less complicated and less bulky as compared to the ordinary rheostat based speed control mechanisms of DC motor drives. Generally there are two different types of PWM techniques may be used to control the speed of DC drives [13], such as (a) variable frequency-constant duty (VFCD) PWM and (b) constant frequency-variable duty (CFVD) PWM. In the first method, the frequency of the controlling signal may be varied keeping the ratio of on and off periods fixed, to vary the average voltage across the DC motor drive. And in the second case, the duty cycle is varied keeping the frequency of the controlling signal fixed to vary the average voltage across the DC motor drive. The second technique requires less complex circuitry to achieve wide range of variations in speed of the DC motors, which intern makes the entire system more cost effective. But the primary disadvantage of the conventional CFVD PWM technique is large abrupt mechanical shocks (kicks) [14] have to be accepted by the rotating armature of a DC motor due to the application of large amplitude narrow pulse trains to achieve very low speed. This fact may result damage to the rotating mechanism of the armature which intern may reduce the life of the DC motor drive. Moreover the transient response the rotating drives are poor due to the presence of only a single controlling parameter, i.e. duty cycle of

the PWM signal [1,2] and absence of any other control to minimize the time required to increase or decrease the speed of the drive within any specified range.

In this paper, the authors have proposed a new method for speed control of DC motors by modifying the conventional CFVD PWM technique via another extra control signal having special sinusoidal form. The extra control signal is subtracted from the conventional fixed amplitude CFVD PWM speed control signal to obtain the modified speed control signal. The proposed modified speed control signal provides gradual periodic increase and decrease in the amplitude of consecutive pulses for all duty cycles. Thus for very low duty cycles (for achieving very low speed) the abrupt mechanical shocks on the armature can be avoided, thereby damage of the armature may be avoided. The peak amplitude of the extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the ordinary PWM signal. A circuit for generating the modified control signal has been designed and fabricated. Finally the experiments are carried out to study the speed control characteristics of a 9 V DC motor by using the proposed method and those are compared with the characteristics obtained from conventional CFVD PWM control technique. The proposed method is found to be better than the conventional CFVD PWM speed control method as regards flexibility in speed control, transient response and abrupt electrical breaking.

The rest of the paper is organized as follows. The next section describes the theoretical background associated with the conventional CFVD PWM based speed control technique in brief along with the proposed technique in detail. The design and fabrication methodologies of the proposed circuit to generate modified PWM signal are discussed in the section 3. The results obtained from the experiments are presented and discussed in the section 4. Finally the paper is concluded in the section 5.

2. THEORY

In this section, initially the conventional method of ordinary CFVD PWM technique for speed control of DC motor drives is discussed in brief. The disadvantages associated with the conventional method are also mentioned. Finally, the proposed method of DC motor speed control via modified CFVD PWM is discussed in detail.

2.1 Conventional CFVD PWM Speed Control Technique

The typical CFVD PWM control signals of constant time period T_c (constant frequency f_c = $1/T_c$) and peak amplitude V_c are shown in Fig. 1 for different duty cycles ($d_c = T_{on}/T_c$; where $T_c = T_{on} + T_{off}$) such as (a) 10%, (b) 30%, (c) 50%, (d) 70% and (e) 90%. Mathematically the conventional CFVD PWM control signal may be expressed as [15]

$$\left.\begin{aligned} v_c(t) = V_c \quad & for\ \ iT_c < t \le (d_cT_c + iT_c) \\ = 0 \quad & for\ \ (d_cT_c + iT_c) < t \le (i+1)T_c \end{aligned}\right\}, \tag{1}$$

where i = 0, 1, 2, 3, …… , etc. Now the average value of the control signal ($v_c(t)$) for duty cycle of d_c may be calculated as

$$V_{av}^{c} = \frac{1}{T_c}\int_{iT_c}^{(i+1)T_c} v_c(t)\,dt = \frac{1}{T_c}\left[\int_{iT_c}^{(d_cT_c+iT_c)} V_c\,dt + \int_{(d_cT_c+iT_c)}^{(i+1)T_c} 0\,dt\right] = d_cV_c\,. \quad (2)$$

Thus the average voltage V_{av}^{c} of the control signal ($v_c(t)$) is directly proportional to the duty cycle (d_c). By changing the value of d_c from 0 to 100%, the average voltage (V_{av}^{c}) can be changed from 0 to V_c. Speed of the DC motor (N in rpm) is directly proportional to V_{av}^{c}. Thus by varying the duty cycle of the control signal, the speed of the DC motor can be varied. But for constant V_c, the speed of the DC motor can only be varied within a single range by varying d_c. Also, due to the inertia of the rotating armature and absence of any additional control over speed other than d_c, sharp rise or decay in speed of the DC drive is very difficult to achieve. Moreover, due to application of train pulses of very small duty cycle ($d_c \leq 10\%$) to run the DC motor in very low rpm for long time, the rotating armature has to accept abrupt mechanical shocks (kicks) consecutively due to applied large amplitude narrow pulse trains, which may cause damage to the armature and consequently reducing the life of the DC motor.

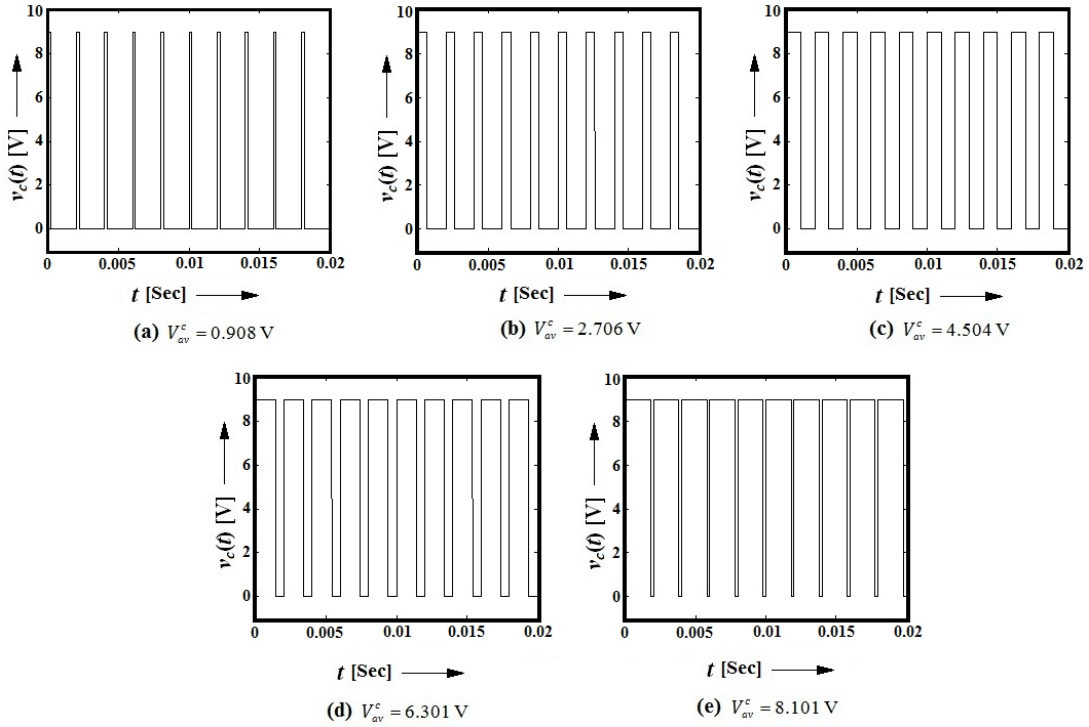

Fig. 1. Typical conventional CFVD PWM control signals of frequency 500 Hz, peak amplitude 9 V for different duty cycles such as (a) 10%, (b) 30%, (c) 50%, (d) 70% and (e) 90%

2.2 The Proposed Technique

In the proposed method, a signal of form given in equation (3) of lower fundamental frequency (i.e. $f_s < f_c$; $\therefore T_s > T_c$) is subtracted from the conventional CFVD PWM speed control signal ($v_c(t)$) to obtain the modified control signal ($v_{sc}(t)$). The said extra control signal is given by

$$v_s(t) = V_s\left[K_s - \sin(2\pi f_s t)\right], \tag{3}$$

where $f_s = 1/T_s$ and T_s is the time period. Thus the modified speed control signal may be expressed as

$$v_{sc}(t) = v_c(t) - v_s(t), \tag{4}$$

where the time domain descriptions of $v_c(t)$ and $v_s(t)$ are given in equations (1) and (3) respectively. The fundamental frequency of the signal $v_s(t)$ is taken to be n-times smaller as compared to the fundamental frequency of $v_c(t)$ (i.e. $f_s = f_c/n$; $\therefore T_s = nT_c$, where n is an integer greater than one). The peak amplitude of the subtracted signal $v_s(t)$ (i.e. V_s) provides an additional control over speed of the DC motor along with the duty cycle (d_c) of the PWM control signal. The abovementioned modified PWM signals are shown in Fig. 2 for different duty cycles and for different V_s/V_c ratio. The mathematical expression of the overall control signal is given by

$$\left.\begin{aligned} v_{sc}(t) &= V_c - V_s\left[K_s - \sin\left(\frac{2\pi t}{nT_c} + \theta_{sc}\right)\right] && for\ \ iT_c < t \le (d_cT_c + iT_c) \\ &= 0 && for\ \ (d_cT_c + iT_c) < t \le (i+1)T_c \end{aligned}\right\}, \tag{5}$$

where $i = 0, 1, 2, 3, \ldots\ldots\ldots\ldots, (n-1)$; θ_{sc} is the initial phase of $v_s(t)$ and K_s is a constant associated with the circuit. The value of θ_{sc} may remains within the range $0 \le \theta_{sc} \le (2\pi/n)$. Now the average value of $v_{sc}(t)$ may be calculated as

$$V_{av}^{sc} = \frac{1}{T_s}\int_0^{T_s} v_{sc}(t)dt = d_c(V_c - K_sV_s) + \frac{V_s}{nT_c}\sum_{i=0}^{(n-1)}\left(\int_{iT_c}^{(d_cT_c+iT_c)} \sin\left(\frac{2\pi t}{nT_c} + \theta_{sc}\right)dt\right). \tag{6}$$

The first term of equation (6) may be varied by varying either d_c or V_s or both simultaneously. The second term of the equation (6) is a function of d_c, V_s, n and θ_{sc} (say $\Theta(d_c, V_c, n, \theta_{sc})$) and $\Theta(d_c, V_c, n, \theta_{sc}) \approx 0$ for $0 \le d_c \le 1.0$, $0 \le n \le 10$ and $0 \le V_s \le 20$ V. Thus by varying d_c, the average control voltage (V_{av}^{sc}) may be varied and consequently the speed of the DC motor may be varied. Moreover, for constant V_c, the peak amplitude of the subtracted signal $v_s(t)$ (i.e. V_s) provides an additional control over V_{av}^{sc} which intern leads to an additional control over the speed of the DC motor.

The average voltage of the overall control signal (i.e. V_{av}^{sc}) becomes negative for

$$\left(\frac{V_s}{V_c}\right) > \left(\frac{nd_cT_c}{nd_cK_sT_c - \Theta}\right) = \frac{1}{K_s} \qquad \left(\because \Theta << nd_cK_sT_c \;\; \forall d_c > 0\right). \tag{7}$$

Thus the direction of the rotation of the DC motor can be reversed by changing the V_s/V_c ratio above the specified value given in equation (7). Faster control over the speed reduction or increment, i.e. better transient characteristics can also be achieved due this additional control mechanism. Electrical breaking of the DC motor can also be achieved by varying V_s for a particular d_c. It can be observed from equation (7) that the abrupt electrical breaking of the 9 V DC motor may be achieved if the value of V_s is abruptly increases just above 14.137 V for $K_s = 2/\pi$, $V_c = 9$ V, $0 \leq d_c \leq 1.0$ and any value of n and T_c. Moreover, for smaller duty cycles ($d_c \leq 10\%$), gradual periodic increase and decrease in the amplitude of the consecutive narrow pulses (Figs. 2 (a) – (d)), possibility of abrupt mechanical shocks on the armature rotating in lower speed may also be avoided, which intern leads to achieve longer life of DC motors.

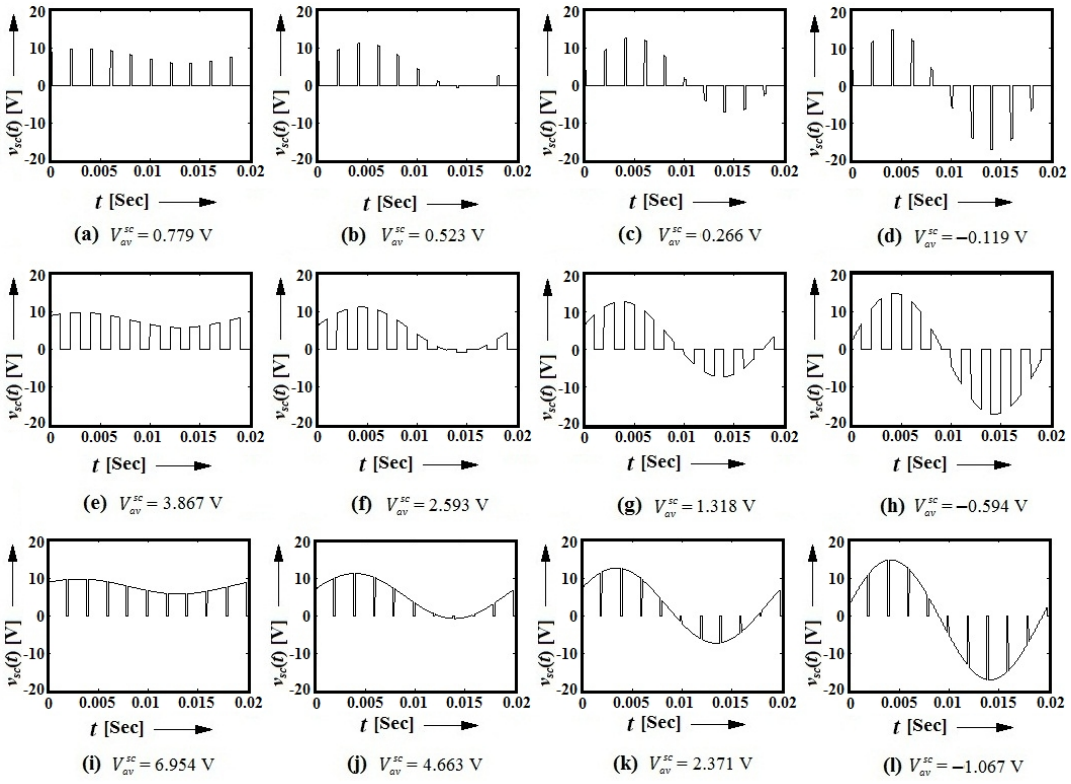

Fig. 2. Typical proposed modified PWM control signals (here n = 10); here the frequency and peak amplitude of the pulse train ($v_c(t)$) are taken to be f_c = 500 Hz and V_c = 9 V respectively; the duty cycles of the pulse train ($v_c(t)$) are taken to be 10% in (a) – (d), 50% in (e) – (h) and 90% in (i) – (l); the V_s/V_c ratio are taken to be 0.22 in (a), (e) and (i), 0.67 in (b), (f) and (j), 1.11 in (c), (g) and (k) and 1.78 in (d), (h) and (l)

3. DESIGN AND FABRICATION OF THE CIRCUIT

The block diagram of the system to generate the proposed modified PWM signal for speed control of DC drives is shown in Fig. 3. At first a circuit capable of generating fixed amplitude CFVD PWM signal ($v_c(t)$) has been designed. The AC main supply voltage (230 V, 50 Hz) has to be stepped down via a centre-tapped step down transformer. Variable amplitude of the sinusoidal signal at the secondary of the transformer may be achieved via a potentiometer (POT) connected across the secondary terminals. The adjustable amplitude sinusoidal signal must be first rectified via a full-wave rectifier and then filtered by using a suitably designed low pass filter (LPF) to obtain the term K_sV_s (where $K_s = 2/\pi$). An analog subtractor circuit may be used to obtain the difference between the terms K_sV_s and $V_s \sin(2\pi f_s t)$, i.e. to construct the extra control signal $v_s(t)$. Finally another analog subtractor circuit may be used to obtain the proposed modified PWM control signal, i.e. $v_{sc}(t) = v_c(t) - v_s(t)$ as shown in Fig. 3.

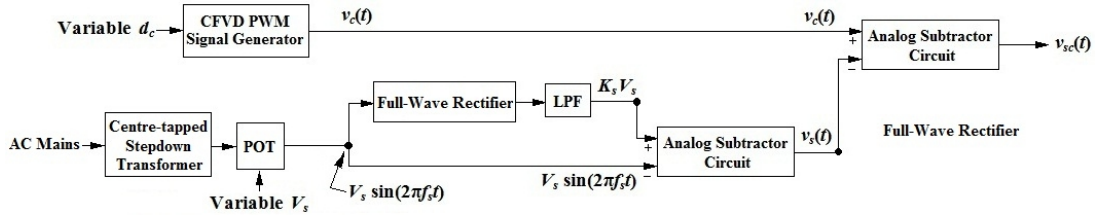

Fig. 3. Block diagram of the system to generate the proposed modified PWM signal

The final designed circuit is shown in Fig. 4. A 555 timer IC based as table multivibrator circuit is used to generate fixed amplitude CFVD PWM signal ($v_c(t)$). The output of this circuit (at pin 3) provides a square-wave of fixed amplitude V_c = 9 V and frequency f_c = 483.09 Hz. The duty cycle of the output square-wave may be varied by adjusting the 10 KΩ potentiometer (POT 1). Three 0.1 μF ceramic disk capacitors are connected in parallel to obtain the desired value of the frequency determining capacitor, i.e. C = 0.3 μF. Say, for a particular position of POT1, the left side of it, i.e. from wiper to the cathode of the diode D1 has the value R_a and similarly the right side of POT1, i.e. from the wiper to the anode of the diode D2 have the value R_b (obviously $R_a + R_b$ = 10 KΩ), then the frequency determining capacitor, i.e. C will be charged from the 9 V DC supply through R_1 = 500 Ω resistor, diode D1 and finally R_a. The capacitor C will be charged up to 2/3 of V_{cc} (i.e. up to 6 V). Thus the total charging time may be easily calculated as $T_{on} = 0.69(R_1 + R_{f1} + R_a)C$ [16], where R_{f1} is the forward resistance of the diode D1. After the complete charging up to $2V_{cc}/3$, the capacitor will discharge through the resistor R_b and diode D2. The discharging will occur until the voltage across the capacitor just falls below $V_{cc}/3$ (i.e. 3 V); after which again the charging will start through the previous path as mentioned earlier. The total discharging period may be calculated as $T_{off} = 0.69(R_b + R_{f2})C$ [16],where R_{f2} is the forward resistance of the diode D2. These charging and discharging processes will be continued repetitively. The time period of the output square-wave is given by $T_c = T_{on} + T_{off} = 0.69(R_1 + R_{f1} + R_{f2} + R_a + R_b)C$. Thus the expressions of frequency and the duty cycle may be written as $f_c = 1/T_c = 1/[0.69(R_1 + R_{f1} + R_{f2} + R_a + R_b)C]$ and $d_c = T_{on}/T_c = (R_1 + R_{f1} + R_a)/(R_1 + R_{f1} + R_{f2} + R_a + R_b)$. If the POT1 is adjusted then both the values of R_a and R_b will change simultaneously, but summation of them will remain always fixed, i.e. $R_a + R_b$ = 10 KΩ. Thus by adjusting POT1, the duty cycle (d_c) will vary accordingly, but the frequency (f_c) will remain unchanged. Therefore the output waveform is the desired CFVD PWM control signal ($v_c(t)$) whose duty

cycle (d_c) may be changed by adjusting the POT1 keeping the frequency of oscillation (f_c) unchanged.

A centre-tapped transformer (T) is used to step down the 230 V, 50 Hz AC main supply to 18 – 0 – 18 V, 50 Hz sinusoidal signal. A 10 KΩ potentiometer (POT2) is connected across the secondary terminals to obtain the adjustable AC voltage amplitude (V_s) at the secondary. A full-wave rectifier circuit comprising of two rectifying diodes (D3 and D4) cascaded with a shunt capacitor (1000 μF) LPF is used to obtain the steady term K_sV_s (here $K_s = 2/\pi$) which is fed at the non-inverting input of the analog subtractor circuit made of IC 741 operational amplifier (biased via V_{CC} = +20 V, V_{EE} = –20 V). The voltage across the POT2 (i.e. $V_s \sin(2\pi f_s t)$) is given as another input to the subtractor circuit at the inverting input terminal. Thus at the output of the will provide the desired extra control signal $v_s(t) = V_s(K_s – \sin(2\pi f_s t))$ with adjustable V_s via POT2, where $K_s = 2/\pi$ and f_s = 50 Hz. Initially the offset nullification of the Op-Amp has been achieved by adjusting the 10 KΩ POT3 as shown in Fig. 4. Another similar analog subtractor circuit finally used to obtain the difference between $v_c(t)$ and $v_s(t)$ to construct the proposed modified CFVD PWM signal $v_{sc}(t) = v_c(t) – v_s(t)$. Finally the proposed control signal ($v_{sc}(t)$) is used to drive the 9 V DC motor as shown in Fig. 4.

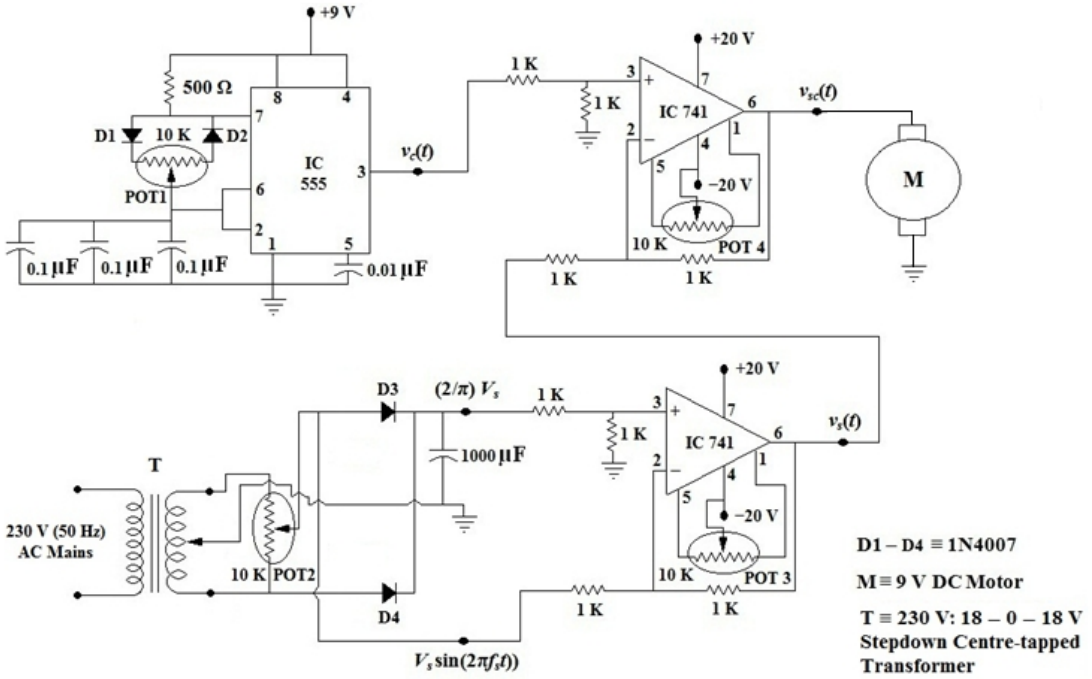

Fig. 4. The final designed circuit to generate the proposed modified PWM signal

The complete PCB layout of the designed circuit has been sketched via "EAGLE 5.10.0 Light" software [17]. After obtaining the layouts, the said PCB has been fabricated via chemical etching procedure [18] and finally the components are carefully soldered on the fabricated PCB to obtain the complete module to carry out experimental measurements.

4. EXPERIMENTAL RESULTS AND DISCUSSION

After fabrication of the designed circuit described in the previous section, the experiments are carried out to study the speed control characteristics of a 9 V DC motor drive via the proposed method and results are compared with those obtained via the conventional CFVD PWM speed control technique. Initially the accuracy of performance of the fabricated circuit has been verified by measuring average voltages of the modified PWM signal (V_{av}^{sc}) at different duty cycles (d_c) of the PWM signal for different peak amplitudes of the extra control signal (V_s). At first the value of V_s has been set at a particular value (any one of 0, 2, 4, 6, 8, 10, 12, 14 and 16 V) by adjusting the POT2 and by observing the waveform of $V_s \sin(2\pi f_s t)$ at the input of the full-wave rectifier section in channel 1 of a digital storage oscilloscope (DSO) display.

For particular value of V_s, the duty cycle of the (d_c) of the PWM signal has been varied from 5 – 95% in a step increment of 5% by adjusting the POT1 at each case and observing the PWM waveform at the pin 3 of IC 555 in channel 2 of the DSO display and for each and every value of d_c the average value of $v_{sc}(t)$ (i.e. V_{av}^{sc}) has been measured by using a DC voltmeter connected across the DC motor (not shown in Fig. 4). Both theoretically (equation (6)) and experimentally obtained variations of average voltage across the 9 V DC motor with duty cycle of the PWM signal for different values of peak amplitude of the extra control signal such as V_s = 0 V, V_s = 2 V, V_s = 4 V, V_s = 6 V, V_s = 8 V, V_s = 10 V, V_s = 12 V, V_s = 14 V and V_s = 16 V are shown in Figs. 5 (a) – (i). Average voltage across the 9 V DC motor for different duty cycle of the PWM signal for different values of peak amplitude of the extra control signal are listed in Table 1. It is interesting to observe from Figs. 5 (a) – (i) and Table 1 that the theoretical and experimental results are close in agreement which intern proves that the accuracy of performance of the fabricated circuit is sufficient. Only some discrepancies (in the order of maximum 8%) between the theoretical and experimental results have been observed for low duty cycles for all values of V_s. But for moderate or higher values of duty cycles the theoretical and experimental results are observed to be in good agreement for all values of V_s. It is also noteworthy that the values of V_{av}^{sc} become negative for all d_c (5 – 95%) while the value of V_s exceeds 14 V. This reversal of sign of V_{av}^{sc} due to V_s > 14 V indicates the change in the direction of rotation of the DC motor drive.

For particular value of V_s, the duty cycle of the (d_c) of the PWM signal has been varied from 5 – 95% in a step increment of 5% by adjusting the POT1 at each case and observing the PWM waveform at the pin 3 of IC 555 in channel 2 of the DSO display and for each and The average current through the DC motor (I_{av0}^{sc}) under no load or free running condition for each and every average voltage across it (V_{av}^{sc}) have been measured by using a DC ammeter connected series with the DC motor drive (not shown in Fig. 4).

The variations of average current through the 9 V DC motor (I_{av0}^{sc}) under no load or free running condition with applied average voltage across it (V_{av}^{sc}) for different values of peak amplitude of the extra control signal such as V_s = 0 V, V_s = 2 V, V_s = 4 V, V_s = 6 V, V_s = 8 V, V_s = 10 V, V_s = 12 V, V_s = 14 V and V_s = 16 V are shown in Figs. 6 (a) – (i). It is observe from Figs. 6 (a) – (i) that for $V_s \leq$ 14 V both the values of I_{av0}^{sc} and V_{av}^{sc} for all d_c values are found to be positive (i.e. quadrant (I) operation), but for V_s > 14 V both the values of I_{av0}^{sc} and

V_{av}^{sc} for all d_c values are found to be negative which indicates the quadrant (III) operation leading to reversal in direction of rotation.

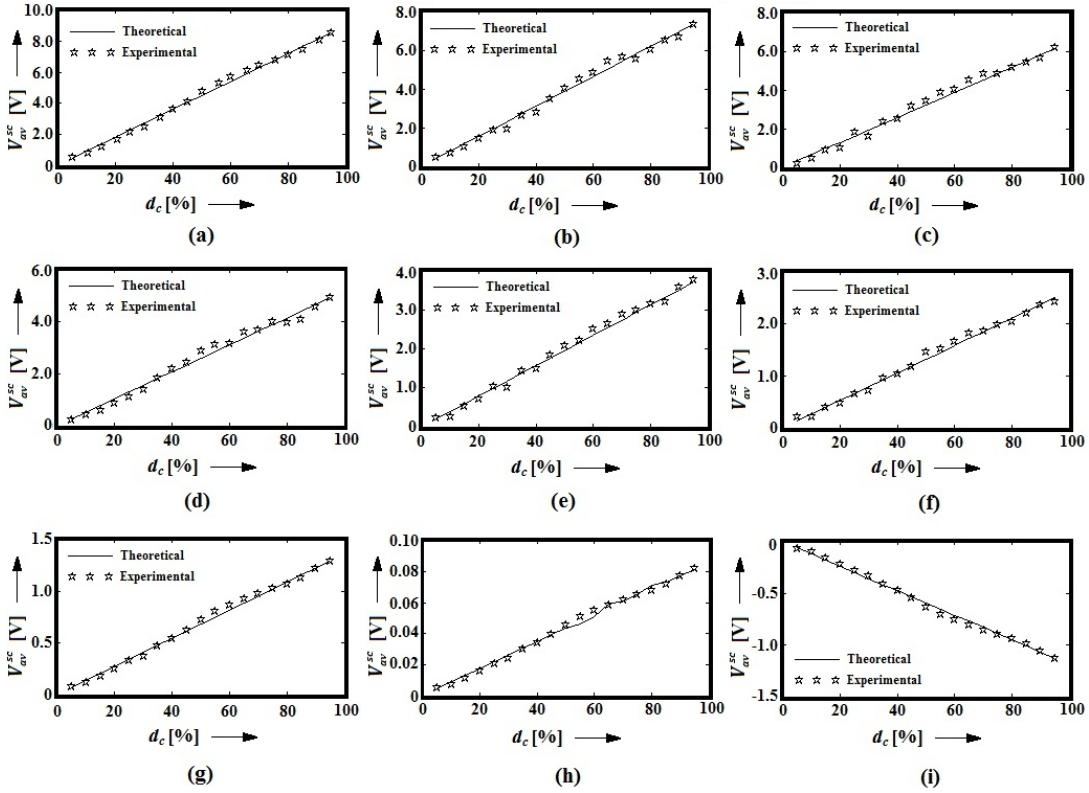

Fig. 5. Variations of applied average voltage across the 9 V DC motor with duty cycle of the PWM signal for different values of peak amplitude of the extra control signal such as (a) V_s = 0 V, (b) V_s = 2 V, (c) V_s = 4 V, (d) V_s = 6 V, (e) V_s = 8 V, (f) V_s = 10 V, (g) V_s = 12 V, (h) V_s = 14 V and (i) V_s = 16 V; here f_c = 483.09 Hz, f_s = 50 Hz and θ_{sc} is chosen to be any random value within the range $0 \leq \theta_{sc} \leq (2\pi/n)$ for each case of theoretical calculation

Variations of no load average current (I_{av0}^{sc}) through the 9 V DC motor drive and applied average voltage across it (V_{av}^{sc}) with peak amplitude of the extra control signal (V_s) for different duty cycles (d_c) of the PWM signal are shown in Fig. 7. It is observed from Fig. 7 that both the I_{av0}^{sc} and V_{av}^{sc} decrease with the increase of V_s for all values of d_c. It is interesting to note from Fig. 7 that signs of both I_{av0}^{sc} and V_{av}^{sc} reversed from positive to negative while the value of V_s increased just above 14.137 V precisely; this value is exactly equal to the critical value of V_s obtained from equation (7) above which the sign reversal of both I_{av0}^{sc} and V_{av}^{sc} occur, i.e. $(V_s)_{Critical} = \pi V_c/2$ = 14.137 V (where V_c = 9 V).

Table 1. Average voltage across the 9 V DC motor for different duty cycle of the PWM signal for different values of peak amplitude of the extra control signal

d_c (%)	V_{av}^{sc} (V)																	
	V_s = 0 V		V_s = 2 V		V_s = 4 V		V_s = 6 V		V_s = 8 V		V_s = 10 V		V_s = 12 V		V_s = 14 V		V_s = 16 V	
	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.	Th.	Pr.
5	0.45	0.50	0.39	0.46	0.32	0.25	0.26	0.33	0.19	0.11	0.13	0.09	0.07	0.07	0.00	0.00	-0.06	-0.06
10	0.91	0.75	0.78	0.49	0.65	0.57	0.52	0.41	0.39	0.23	0.27	0.18	0.13	0.11	0.00	0.00	-0.12	-0.09
15	1.35	1.16	1.16	1.24	0.97	0.82	0.78	0.43	0.58	0.34	0.39	0.30	0.20	0.17	0.01	0.00	-0.18	-0.15
20	1.81	1.66	1.55	1.77	1.29	1.04	1.04	1.06	0.78	0.73	0.52	0.58	0.27	0.25	0.02	0.01	-0.24	-0.21
25	2.25	2.15	1.93	1.79	1.61	1.23	1.29	1.29	0.98	0.91	0.66	0.61	0.34	0.32	0.02	0.01	-0.29	-0.28
30	2.70	2.47	2.32	2.06	1.94	1.69	1.55	1.41	1.17	1.15	0.79	0.67	4.09	0.37	0.03	0.02	-0.36	-0.32
35	3.16	3.10	2.71	2.72	2.26	2.23	1.81	1.85	1.37	1.34	0.92	0.88	0.47	0.46	0.03	0.02	-0.42	-0.40
40	3.60	3.59	3.09	3.18	2.58	2.72	2.08	2.17	1.56	1.69	1.05	1.04	0.55	0.54	0.03	0.03	-0.47	-0.47
45	4.05	4.11	4.48	3.59	2.90	2.84	2.33	2.46	1.76	1.81	1.19	1.20	0.61	0.62	0.04	0.03	-0.53	-0.54
50	4.50	4.78	3.86	3.93	3.22	3.52	2.59	2.79	1.95	1.96	1.31	1.31	0.68	0.72	0.04	0.04	-0.59	-0.63
55	4.95	5.32	4.25	4.63	3.55	4.13	2.84	3.01	2.15	2.34	1.45	1.64	0.74	0.81	0.05	0.05	-0.65	-0.70
60	5.40	5.72	4.63	5.16	3.87	4.15	3.11	3.30	2.34	2.49	1.58	1.70	0.81	0.86	0.05	0.05	-0.71	-0.75
65	5.85	6.12	5.02	5.29	4.19	4.37	3.36	3.33	2.54	2.59	1.71	1.82	0.88	0.92	0.06	0.05	-0.77	-0.81
70	6.30	6.48	5.40	5.35	4.51	4.63	3.62	3.67	2.73	2.83	1.84	1.95	0.95	0.97	0.06	0.06	-0.82	-0.85
75	6.75	6.80	5.79	5.58	4.84	4.99	3.88	3.89	2.93	2.97	1.97	2.00	1.02	1.02	0.07	0.06	-0.89	-0.89
80	7.19	7.10	6.18	6.27	5.16	5.28	4.14	4.10	3.12	3.09	2.10	2.11	1.08	1.07	0.07	0.07	-0.95	-0.93
85	7.65	7.48	6.56	6.41	5.48	5.49	4.40	4.37	3.32	3.22	2.23	2.21	1.15	1.13	0.07	0.07	-1.00	-0.98
90	8.09	8.06	6.95	6.81	5.81	5.60	4.66	4.61	3.51	3.57	2.36	2.33	1.22	1.22	0.08	0.07	-1.07	-1.06
95	8.54	8.54	7.33	7.57	6.12	6.24	4.92	4.99	3.71	3.68	2.50	2.48	1.29	1.29	0.08	0.08	-1.13	-1.12

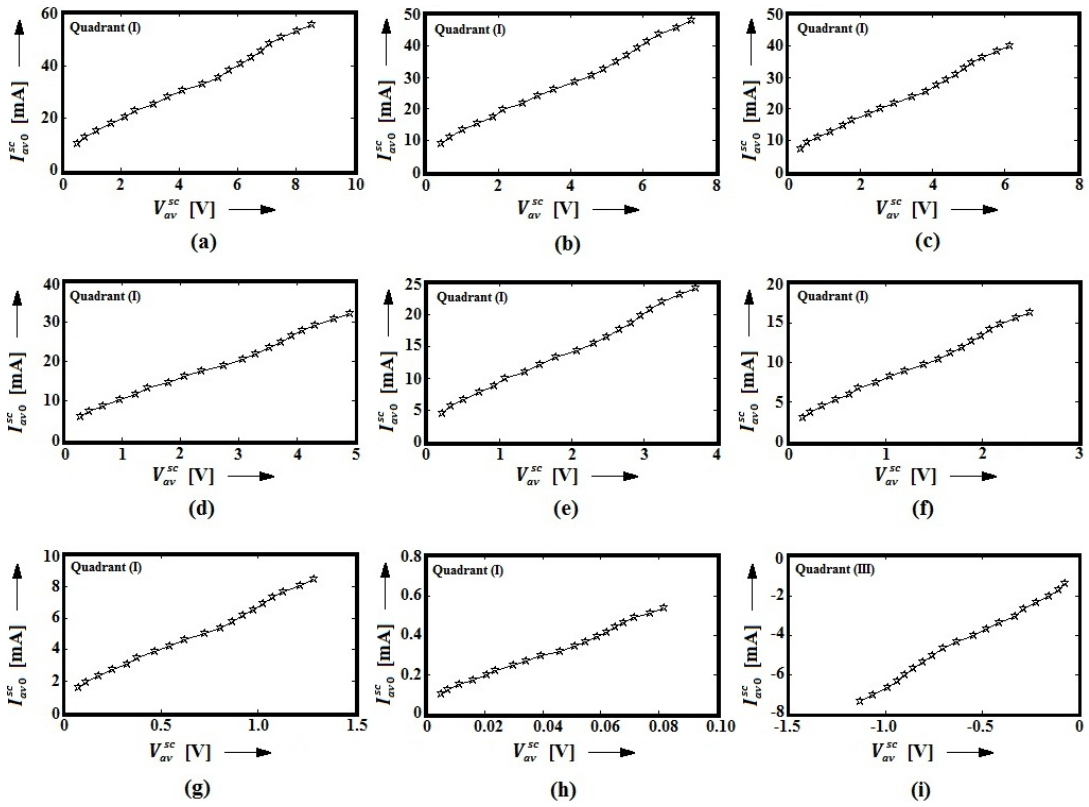

Fig. 6. Variations of average current through the 9 V DC motor under no load or free running condition with applied average voltage across it for different values of peak amplitude of the extra control signal such as (a) V_s = 0 V, (b) V_s = 2 V, (c) V_s = 4 V, (d) V_s = 6 V, (e) V_s = 8 V, (f) V_s = 10 V, (g) V_s = 12 V, (h) V_s = 14 V and (i) V_s = 16 V

The speed of the 9V DC motor (N) in rpm under no load condition has been measured at different duty cycles (d_c) of the PWM signal for different peak amplitudes (V_s) of the extra control signal via a photo-contact tachometer (model DT-205L [19]). Photo-contact tachometer enables direct rpm measurements sensed from an easy to aim visible light beam directed toward a rotating shaft without mechanical contact; leading to more precise measurement of speed of the rotating shaft of the DC motor under no load or free running condition. Variations of speed of the DC motor under no load condition with duty cycles of the PWM signal for different peak amplitudes of the extra control signal and with peak amplitude of the extra control signal for different duty cycles of the PWM signal are shown in Fig. 8. It is interesting to observe from Fig. 8 (a) that the parameter V_s provides an extra control over speed along with the d_c. The range of the speed (in rpm) of the DC motor (i.e. starting from minimum speed (N_{min}) up to the maximum speed (N_{max})) may be selected by selecting the corresponding value of V_s (easily obtainable from Fig. 8 (a)) and the speed of the DC drive may be varied from the selected N_{min} to N_{max} by varying the duty cycle (d_c) of the PWM control signal. Moreover, it is observed from Fig. 8 (b) that the electronic breaking of the rotating DC motor drive rotating in any speed (i.e. for any fixed $d_c > 0$) may be achieved by abruptly changing the value of V_s just above critical value of it, i.e. $(V_s)_{Critical}$ = 14.137 V for which the speed of rotation will be either zero or its direction will be reversed.

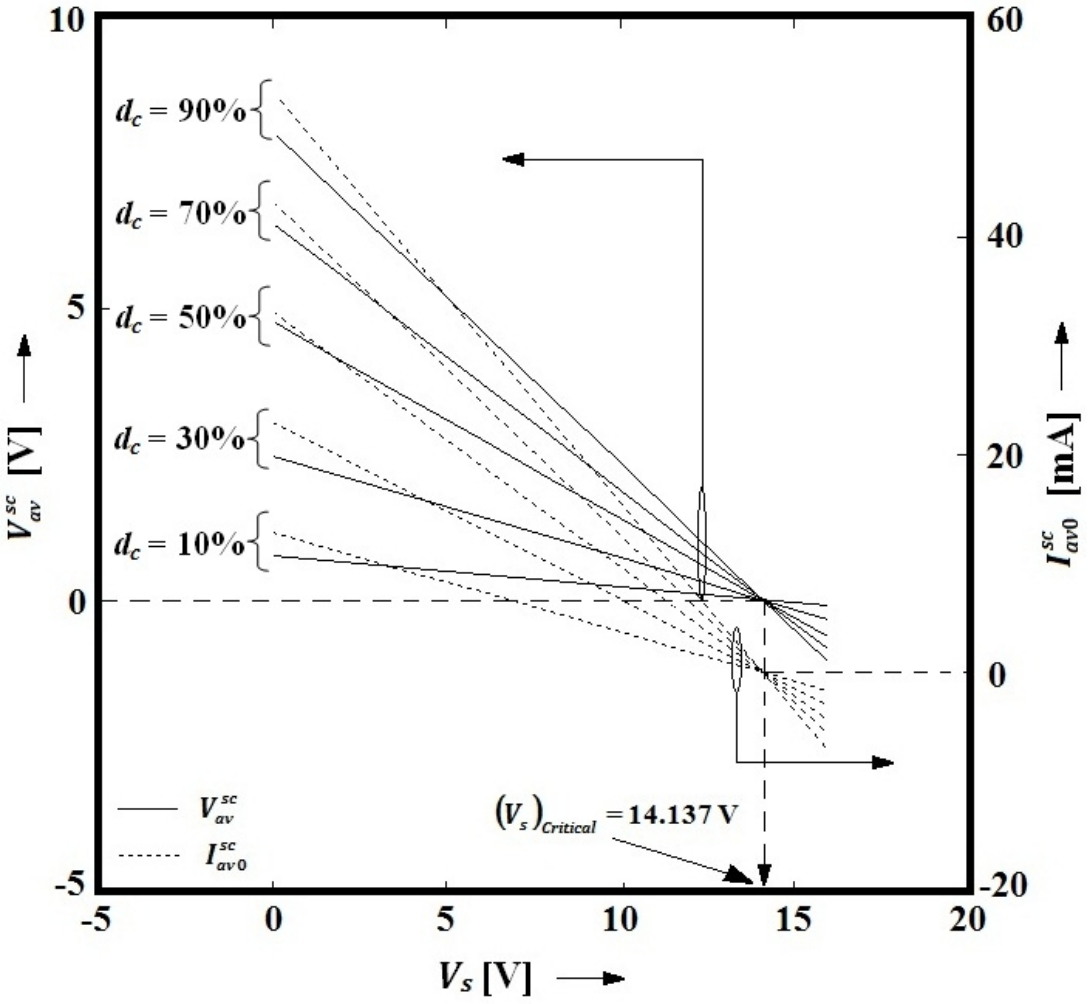

Fig. 7. Variations of no load average current through the 9 V DC motor and applied average voltage across it with peak amplitude of the extra control signal for different duty cycles of the PWM signal

Two types of electronic breaking characteristics of the 9 V DC motor drive are studies by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed as well as by abruptly varying d_c from 90% to 10%, keeping V_s fixed and the results are given in Tables 2 and 3 respectively. This comparative study is carried out to ensure the superiority of the proposed method as compared to the conventional one as regards the abrupt electronic breaking. For each of the abovementioned cases the time required for achieving the steady state minimum speed, i.e. breaking time (t_b) have been measured for five times via a precise online stopwatch [20] and finally average value of t_b has been calculated for each case. A comparative study of both the said electronic breaking methods from Table 2 and 3 reveals that the electronic breaking by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed is more shaper and takes less breaking time (nearly 45% reduction in average breaking time is achieved) as compared to its other counterpart.

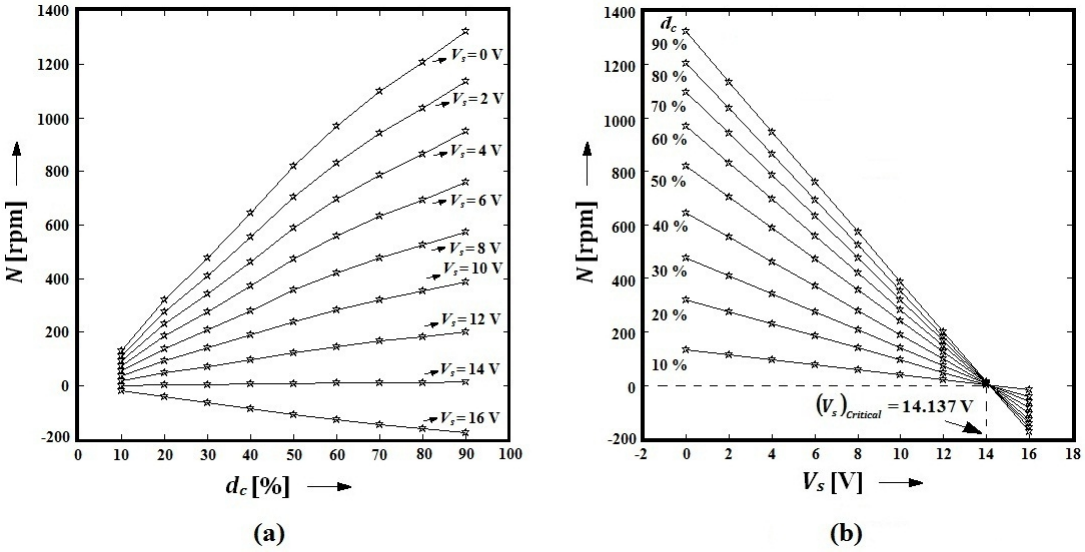

Fig. 8. Variations of speed of the DC motor under no load condition (a) with duty cycles of the PWM signal for different peak amplitudes of the extra control signal and (b) with peak amplitude of the extra control signal for different duty cycles of the PWM signal

Table 2. Electronic breaking characteristics by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed

d_c (%)	N_{max} (rpm)	N_{min} (rpm)	t_b (ms)
90	1323.60	0	511
80	1207.00	0	497
70	1098.50	0	463
60	970.25	0	447
50	819.82	0	427
40	644.89	0	395
30	478.13	0	341
20	320.99	0	278
10	130.96	0	167

Table 3. Electronic breaking characteristics by abruptly varying d_c from 90% to 10%, keeping V_s fixed

V_s (V)	N_{max} (rpm)	N_{min} (rpm)	t_b (ms)
0	1323.60	131.00	1059
2	1136.40	112.40	941
4	949.03	93.90	872
6	761.83	75.38	797
8	574.47	56.84	651
10	387.26	38.32	602
12	199.99	19.79	523
14	12.68	1.25	498
16	-174.51	-17.27	474

The transient speed control characteristics of the DC motor drive under test have been studied for different speed ranges such as 0 – 100, 100 – 300, 300 – 500, 500 – 700, 700 – 900, 900 – 1100 and 1100 – 1300 rpm. The settling times (t_s) have been measured via precise online stopwatch [20] for each of the above mentioned ranges during both speed rise and decay by either varying d_c, keeping V_s fixed or varying V_s, keeping d_c fixed. Average settling time ($\hat{t}_s$) for each case has been calculated from five consecutive measurement data corresponding to that. It is noteworthy from Figs. 9 (a) and (b) that average settling times ($\hat{t}_s$) for each of the ranges under consideration during both speed rise and decay are found to be smaller when the V_s is varied keeping d_c fixed as compared to when d_c is varied keeping V_s fixed. Thus the transient speed control characteristics via the extra control parameter V_s are found to be better as compared to the direct control parameter d_c.

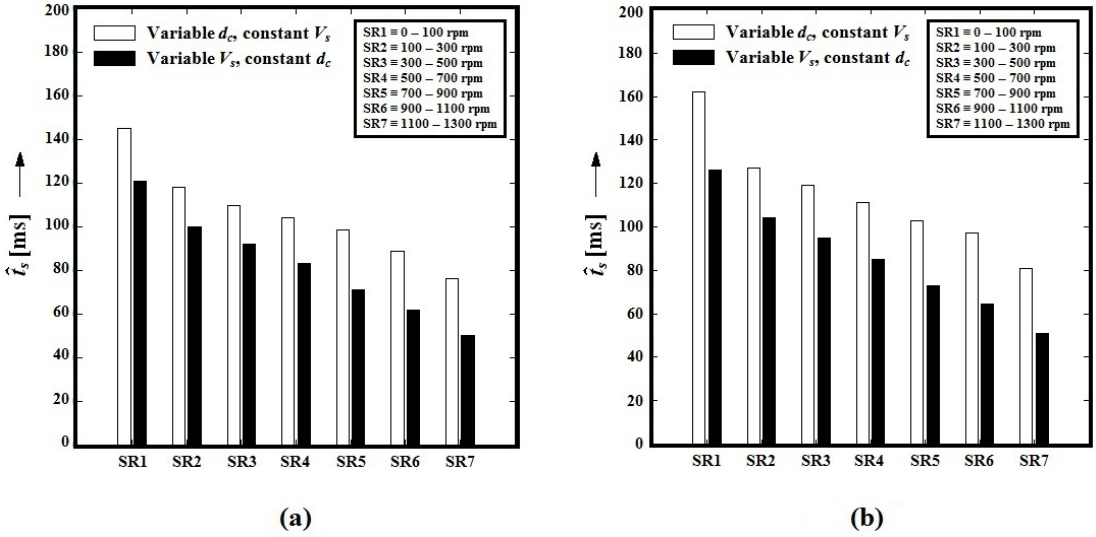

Fig. 9. Bar graphs showing the average settling times for different speed ranges when the duty cycle of the PWM signal is varied keeping the peak amplitude of the extra control signal fixed and when the peak amplitude of the extra control signal is varied keeping the duty cycle of the PWM signal fixed; (a) during speed rise, (b) during speed decay

5. CONCLUSION

A new method for the speed control of DC motor drives via modified CFVD PWM technique has been proposed in this paper. An extra control signal having modified sinusoidal form is subtracted from the conventional fixed amplitude CFVD PWM signal to obtain the modified speed control signal. The peak amplitude of the subtracted extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the ordinary PWM signal. An electronic circuit for generating the modified control signal for 9 V DC motor drive has been designed and fabricated and the experiments are carried out to study the speed control characteristics of the 9 V DC motor under test. In average, around 20 ms smaller settling time during rise or decay of speed for different speed range has been achieved by changing the peak amplitude of the extra control signal keeping duty cycle fixed as compared to changing the duty cycle keeping peak amplitude of the extra control signal

fixed, which in turn shows better transient response of the proposed method than its conventional counterpart. Abrupt electronic breaking has been achieved by increasing the peak amplitude of the extra control signal just above 14.137 V in step, which is in exact agreement with the theoretical calculation presented in the paper. By using the proposed method, around 45% reduction in average breaking time has been achieved as compared to the conventional CFVD PWM speed control technique. Thus the proposed method is found to be better than its conventional CFVD PWM counterpart as regards flexibility in speed control, transient response and abrupt electrical breaking.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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